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Kenneth E. Behring Center

Guide to the GTE Burst Switch Collection

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Collection Overview

Repository:	Archives Center, National Museum of American History
Title:	GTE Burst Switch Collection
Identifier:	NMAH.AC.0833
Date:	1984-1999.
Extent:	7 Cubic feet (14 boxes, 6 map-folders)
Creator:	Information, Technology and Society, Div. of (NMAH, SI). GTE Laboratories Inc.
Language:	English
Summary:	Drawings, patents, notes, computer printouts, articles, and technical papers documenting the GTE Burst-switch; also, subject files relating to many aspects of the burst switch project.

Administrative Information

Acquisition Information

The collection was donated by Thomas Muldoon on December 17, 1999.

Ownership and Custodial History

The collection was transferred to the Archives Center from the Division of Information, Technology & Society on February 22, 2003.

Processing Information

Processed by Alison Oswald, archivist, 2003.

Preferred Citation

GTE Burst Switch Collection, 1984-1999, Archives Center, National Museum of American History.

Restrictions on Access

Collection is open for research and access on site by appointment.

Terms Governing Use and Reproduction

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Historical

The burst switch was developed in the 1970s-1980s at the GTE Laboratories in Waltham, Massachusetts. The burst switch was one of the first switches to demonstrate how voice and data traffic could be integrated into a single network and be handled simultaneously. It was never manufactured on a large scale, but concepts derived from the technology have been used in numerous forms of telecommunications equipment.

Scope and Contents

The collection is arranged into ten series—articles and papers, patents, manuals and instructional guides, testing materials, notes, subject files, software/hardware information, Datacon wire wrap listings, drawings, and 5" and 8" floppy diskettes documenting the GTE burst-switch project. The majority of the project work was done in the early 1980s and continued through 1985. The subject files are arranged alphabetically and relate to specific aspects of the project. The drawings are divided into original and copies. The originals drawings are mylar or vellum. The Mark IIA refers to the final research model of the burst switch.

Arrangement

The collection is divided into ten series.

Series 1: Articles and Papers, 1983-1999

Series 2: Patents, 1987

Series 3: Manuals and Instruction Guides, 1987-1990

Series 4: Testing Materials, 1985-1987

Series 5: Notes, 1985-1988

Series 6: Subject Files, 1985-1991

Series 7: Software/Firmware, 1987-1989

Series 8: Datacon Wire Wrap Listings, 1985-1987

Series 9: Drawings, 1984-1987

Series 10: Floppy disks, 1987-1991

Names and Subject Terms

This collection is indexed in the online catalog of the Smithsonian Institution under the following terms:

Subjects:

Electric switchgear
Telecommunication

Types of Materials:

Drawings -- 1980-2000
Manuals
Notes
Patents -- 20th century
Software

Container Listing

Series 1: Articles and Papers, 1983-1999

Subseries 1.1: Articles, 1983-1999

Box 1	Burst switch Articles, 1983-1999

1.2: Papers, 1984-1986

Box 1	Jack, C.M. Confidence Intervals for the Burst Switched Ring Network Computer Simulation, 1984
Box 1	Jack, C.M. Performance Analysis of Superchannels in a Burst-Switched Integrated Voice/Data Network, 1985
Box 1	Jack, C.M. and Morse, J.D. Simulation and Performance Evaluation of Hub Switch Traffic Congestion, 1985
Box 1	Jack, C.M. and Morse, J.D. Simulation of a Burst Switched Integrated Voice and Bulk Data Communications Network, 1986

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Series 2: Patents, 1987

Box 1	U.S. Patent #4,644,529, High-Speed Switching Processor for a Burst-Switching Communications Systems, 1987
Box 1	U.S. Patent #4,646,294,High-Speed Queue Sequencer for a Burst-Switching Communications System, 1987
Box 1	U.S. Patent #4,698,799, Link Switch for a Burst-Switching Communications System, 1987
Box 1	U.S. Patent #4,698,803, Burst-Switching Communications System, 1987
Box 1	U.S. Patent 4,698,841, Methods of Establishing and Terminating Connections in a Distributed-Control Burst Switching Communications System, 1987
Box 1	U.S. Patent #4,703,478, Burst-Switching Methods for an Integrated Communications System, 1987
Box 1	U.S. Patent #4,707,825, Methods of Installing and Assigning Control Processors in a Distributed-Control Communications System, 1987
Box 1	U.S. Patent # 4,710,916, Switching Apparatus for Burst-Switching Communications System, 1987

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Series 3: Manuals and Instruction GUides, 1987-1990

Box 2	Switch Hardware Manual, 1987
Box 2	In Switch Hardware Manual, 1990
Box 2	Network 911 Service Initializing the Demonstration, 1990
Box 2	Comparison of Interprocessor Communication techniques for a Burst Switch, 1989
Box 2	Initializing and Demonstrating Services on the Exploratory Intelligent Network Testbed, 1991

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Series 4: Testing Materials, 1985-1987

Box 2	Test Log, August 12, 1986 to December 10, 1986
Box 2	Test Log, December 10, 1986 to March 12, 1987
Box 2	Test Log, 1987
Box 2	Bench Test Procedure for Burst Switch Project (HOP bench test), 1986
Box 2	Analog Line Card Bench Test, 1986
Box 2	Data Line Card Bench Test, 1986
Box 2	Frame Test, 1986
Box 2	HSE Bench Test, 1986
Box 2	Test Forms, 1986

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Notes, 1985-1988

Box 10	Burst Trunk Notes, 1987-1988
Box 10	Burst Switch #1, 1985
Box 10	Burst Switch #2, 1985

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Series 6: Subject Files, 1985-1991

Box 10	Analog Line (history file)
Box 10	Analog Line Card, 1987
Box 10	Analog Trunk Card, 1986-1987
Box 10	Analog Trunk, 1987
Box 10	Back Plane (history file)
Box 10	Board Trace Forms, 1985-1987
Box 11	Board Change Descriptors, 1987
Box 11	Burst Switch Project pending Tasks, 1986
Box 11	Burst Switch Micro Code (non-channelized current version, 1987
Box 11	Call Processor, 1987
Box 11	Character Memory, 1987
Box 11	Charles River Museum of Industry, 1990-1991
Box 11	Data Card Line, 1987
Box 11	Datacon Wire Wrap Information, 1987
Box 13	Datacon The Wire Wrapper, empty binder
Box 11	HSE (#120120), 1987
Box 13	Hub Switch/HOP Micro-Code, 1987
Box 11	Inventory, 1985
Box 13, Folder 3	ISO Board Information, 1986-1987
Box 11, Folder 12	Link Alignment Redesign, 1987
Box 11	Link Alignment Redesign (notes), 1987

Box 13	Link Alignment Rewire, 1986
Box 11	Link Switch (history), 1985
Box 11	MARK II A, 1987
Box 12	Micro-Code Assembler Information, 1987
Box 12	Opto Isolator, 1986
Box 12	Queue Sequencer, 1985-1987
Box 12	Relay Panel, 1986
Box 12	Switch Processor (history file), undated
Box 12	Switching Processor—TIP, 1988
Box 12	Switching Processor, undated
Box 12	Release Forms (for hardware), 1987
Box 12	Test jigs and Displays, 1986

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Series 7: Software/Firmware, 1987-1989

Box 3, Folder 1-4	Call Processor Software Listing, Version C, May 27, 1987
Box 4, Folder 1-3	Call Processor Software Listing, Version C, May 27, 1987
Box 5, Folder 1	Burst-Switch Test Firmware, Before 1987
Box 5	Burst-Switch History/Firmware Listings,, Before 1987
Box 5	Burst Trunk Firmware, December 1987
Box 5	Burst Switch Firmware Normal Operatio, November 1987
Box 6, Folder 1-6	Call Processor Version 2.5, August 17, 1989 August 17
Box 7, Folder 1-3	Call Processor Version 2.5, August 1, 1989 August 1

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Series 8: Datacon Wire Wrap Listings, 1985-1987

Box 8, Folder 1	HSE Reset Switch, January 1985
Box 8	Smart Processor I, May 1985
Box 8	Switch Processor, September 1985
Box 8	T1 Interface, September 1985
Box 8	Character Memory, September 1985
Box 8	Queue Sequence, October 1985
Box 8	Data Line Card, January 1986
Box 8	Analog Line/AL1-001, January 1986
Box 8	Analog Card Trunk, February 1986
Box 9	Analog Line/Al1-001, March 1986
Box 9	Switch Processor, June 1986
Box 9	Link Alignment Redesign Board Wrap File, August, 1987
Box 9	Mark IIA, August, 1987
Box 9	New Link Alignment Wrap, Revision A, September, 1987

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Series 9: Drawings , 1984-1987

Subseries 9.1: Originals Drawings, 1984-1987

Map-folder 1	Data line Card Common Circuits, 1985
Map-folder 1	Switching Processor, Sequencer, Microprogram, Prom and Pipeline Register, 1984
Map-folder 1	Mark IIA HSE, 1985
Map-folder 2	Call Processor, 1987
Map-folder 2	Analog Trunk Card, 1985-1986
Map-folder 2	Analog Line Card Circuit 0, 1985
Map-folder 3	Character Memory Board, 1984
Map-folder 3	Switching Processor—TIP, Sequencer, Microprogram, Prom and Pipeline Register, 1984
Map-folder 3	Switching Processor—HOP, Sequencer, Microprogram, Prom and Pipeline Register, 1984
Map-folder 4	Opto-Isolator Card Layout, 1987
Map-folder 4	Opto-Isolator Card, 1987
Map-folder 4	Link Alignment Redesign Board Layout, undated
Map-folder 4	Queue Sequencer, 1984
Map-folder 4	Link Alignment Redesign, 1987

Subseries 9.2: Copies of Drawings, 1984-1987

Map-folder 5	Call processor, 1987
Map-folder 5	Analog Line Card Circuit 0, 1985
Map-folder 5	Analog Trunk Card, 1985-1986
Map-folder 5	Data Line Card (Common Circuits), 1985

Map-folder 5	Switching Processor, Sequencer, Microprogram, Prom and Pipeline Register, 1984
Map-folder 6	Mark IIA Link Switch, 1984-1985
Map-folder 6	Character Memory Timing, 1984-1985
Map-folder 6	Switching Processor Block Diagram, 1984-1985
Map-folder 6	Queue Sequencer Block Diagram, 1984-1985
Map-folder 6	Mark IIA Block Diagram, 1984-1985
Map-folder 6	Link Alignment Redesign Board Layout, undated
Map-folder 6	Link Alignment Redesign Revision A, 1987
Map-folder 6	Queue Sequencer, 1984
Map-folder 6	Character Memory Board, 1984

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Series 10: Floppy Disks (Backup), 1987-1991

Box 14	Burst Switch Assembler, Source, Object, Switching Processors and Debugger, 1987-1988
Box 14	DebuggerZ80, 1989
Box 14	LAB PC's, 1990-1991
Box 14	IP Back-up, 1991

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